



Serial No. 09/785,006

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Aaron M. Schoenfeld
Serial No.: 09/785,006
Filed: February 16, 2001
Title: GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS

Examiner: Unknown
Group Art Unit: Unknown
Docket: 303.259US3

Handwritten notes: 14/Supp, Re. Amend B, Argued, 5/31/01

SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

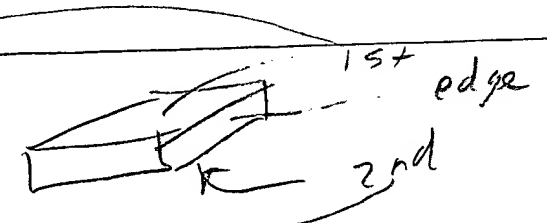
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Before taking up the above-identified application for examination, please enter the following amendments.

IN THE CLAIMS

Please cancel claims 1, 8, and 10 without prejudice or disclaimer. Please add the following new claims:

11. (New) A semiconductor die comprising:
a first planar surface having circuitry thereon;
a second planar surface opposite the first planar surface;
one or more perimeter edges disposed between the first planar surface and the second planar surface; and
at least a portion of at least one perimeter edge of the semiconductor die having a substantially flat surface, the portion extending from the first planar surface to the second planar surface.
12. (New) The semiconductor die as recited in claim 11, wherein each perimeter edge has an entirely flat, smooth surface.
13. (New) The semiconductor die as recited in claim 11, wherein the semiconductor die has a substantially rectangular shape.



Handwritten notes: Sub, DI, B1